What is claimed is :

1. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant over a semiconductor substrate which have gone through predetermined processes;

forming sequentially a first metal layer and a poly-silicon layer over the dielectric layer;

forming an upper electrode pattern by pattering the poly-silicon layer and the first metal layer;

forming a second metal layer covering the upper electrode pattern on an entire surface of the semiconductor substrate; and

forming an upper electrode constituted with the second metal layer, the poly-silicon layer and the first metal layer by patterning the second metal layer so that the second metal layer is connected with the first metal layer.

2. The method as recited in claim 1, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.

3. The method as recited in claim 2, wherein the TiN layer is formed by performing a chemical vapor deposition

(CVD) process.

4. The method as recited in claim 3, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.

5. The method as recited in claim 1, wherein the second metal layer is constituted with one of such layers as a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.

6. The method as recited in claim 5, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000 Å.

7. The method as recited in claim 1, wherein a thickness of the poly-silicon layer ranges from about 300 Å to about 2500 Å.

8. The method as recited in claim 1, wherein the dielectric layer is constituted with one of such layers as a tantalum oxide (Ta_2O_5) layer, a titanium oxide (TiO_2) layer, an aluminum oxide (Al_2O_3)-tantalum oxide (Ta_2O_5) double layer, strontium titanium oxide ($SrTiO_3$) layer and a piezoelectric translator (PZT) layer.

9. The method as recited in claim 1, further

comprising the steps of:

forming an inter-layer insulation film on an entire surface of the semiconductor substrate after forming the upper electrode; and

forming a contact hole exposing a portion of the upper electrode by etching the inter-layer insulation film.